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H02H 3/093

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(56) Documents cited
GB 2244183 A GB 2020124 A GB 1594112 A
GB 1069626 A EP 0253009 A1 EP 0245819 A2
US 4000446 A

(58) Field of search
UK CL (Edition K) H2K KHB KJE KJG
INT CL[5] H02H 3/093

(54) **Circuit breaker with level detectors and timers**

(57) A circuit breaker includes an electronic trip device which responds to sputtering arc-type faults. Level detectors 47, 49, 51 compare the current in the protected circuit to a plurality of threshold levels, and timers, R89, C91 etc time the intervals that the current remains above each threshold, with the threshold levels and intervals selected to generate a response envelope for a trip signal which approximates, with a selected margin, the response of the protected circuit to introduction of a selected inductive load such as a motor into the circuit. If the sensed current falls below a threshold level which was being timed, the associated timer is not cleared unless the current falls below the lowest threshold, so that if the sensed current increases above the associated threshold, timing resumes where it left off. Digital timers may be used instead of analogue ones (Fig 3).

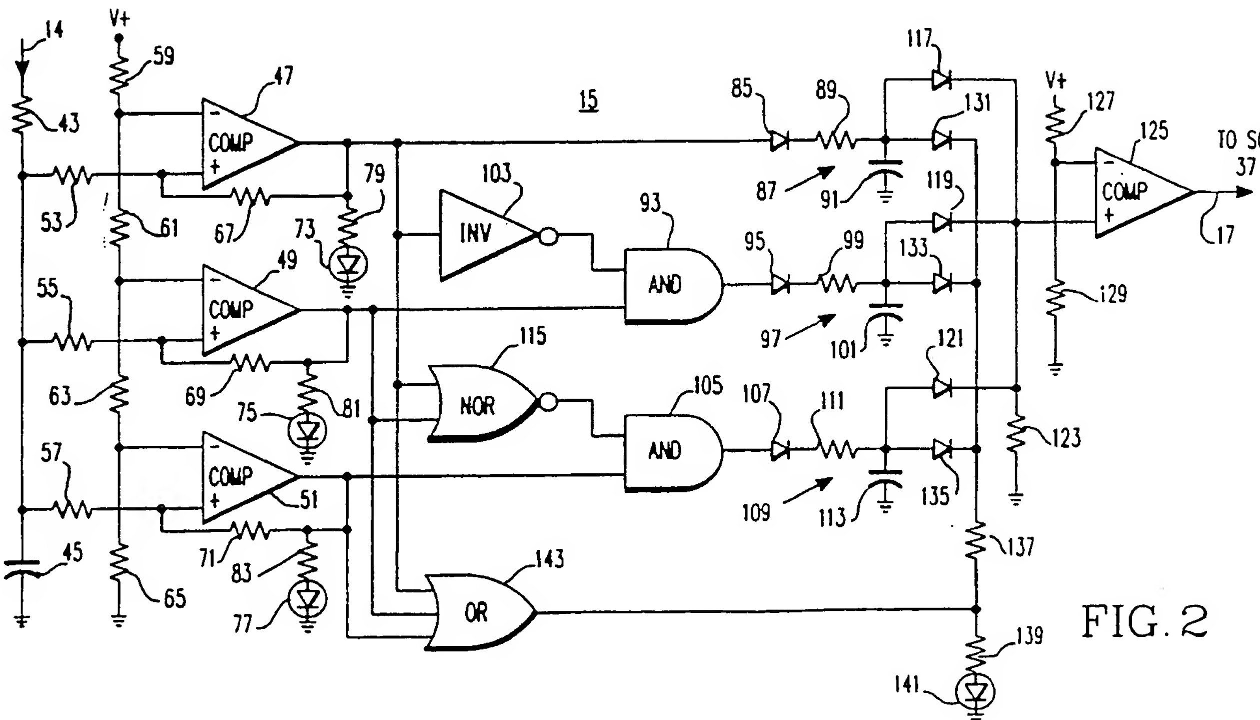
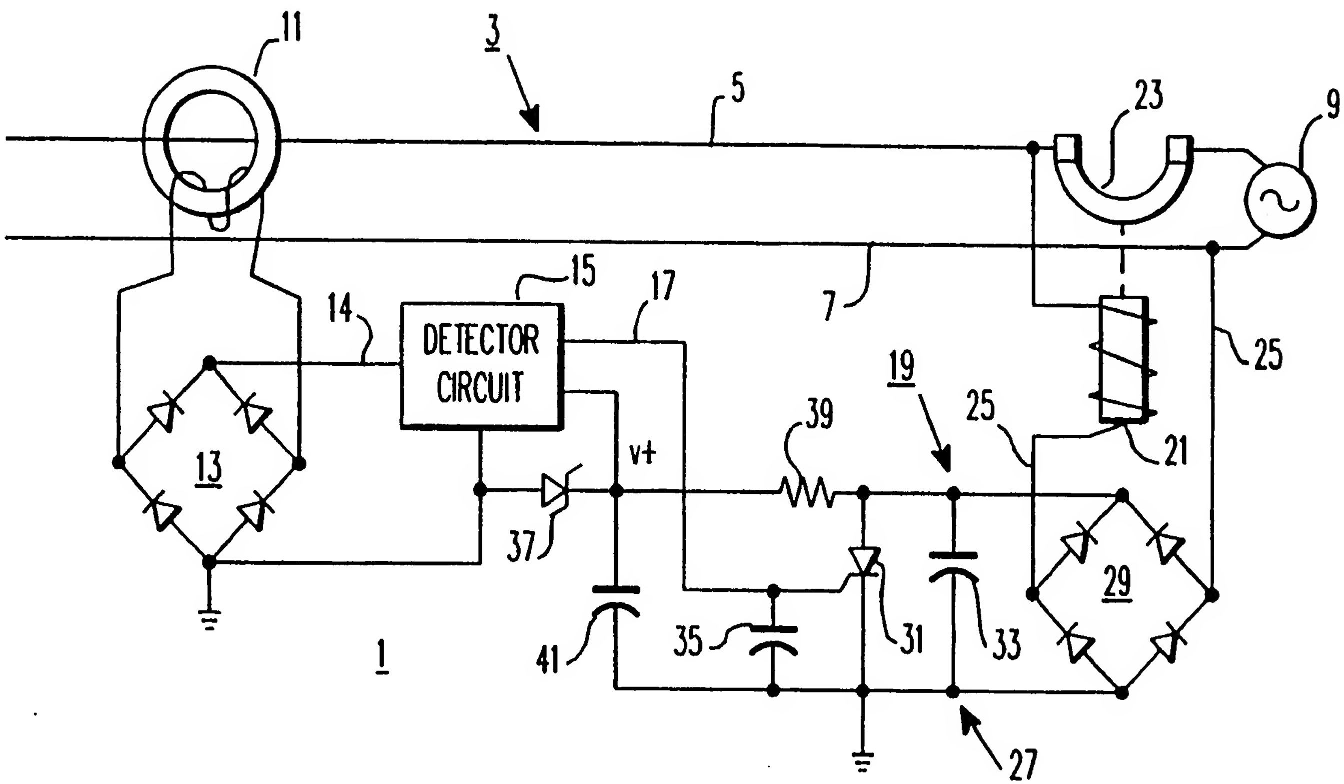


FIG. 2

GB 2 260 042 A



11
3
5
23
9
15
17
14
DETECTOR CIRCUIT
7
19
25
25
39
21
13
v+
29
37
31
33
35
41
1
27

FIG. 1

2/3

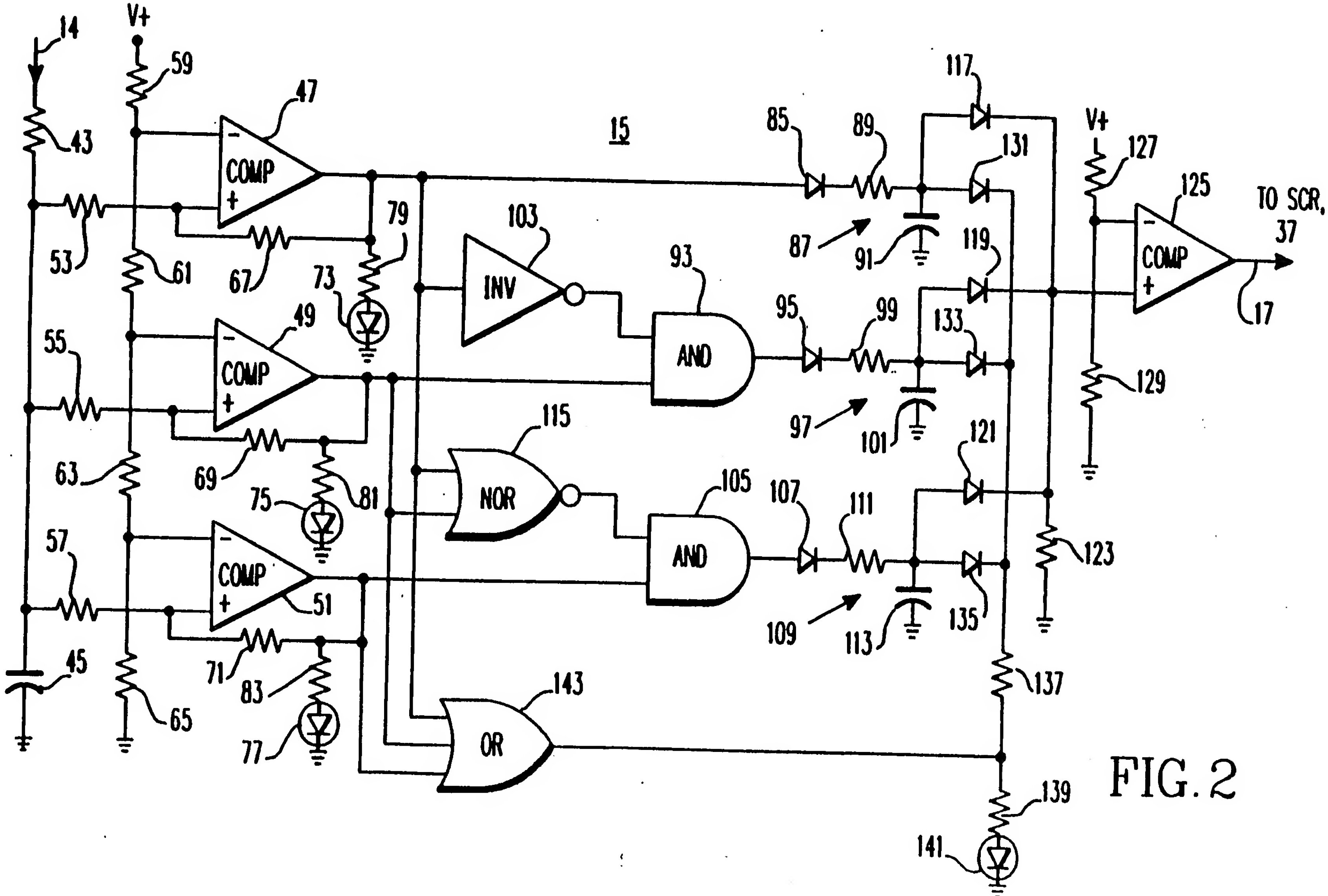

14
V+
59
47
43
53
COMP
COMP
COMP
61
67
79
73
103
INV
93
AND
49
55
63
69
75
81
115
NOR
105
AND
57
51
71
83
77
45
65
143
OR
15
85
89
117
131
87
91
119
95
99
133
97
101
121
107
111
109
113
135
137
139
141
V+
127
125
TO SCR, 37
17
129
123

FIG. 2

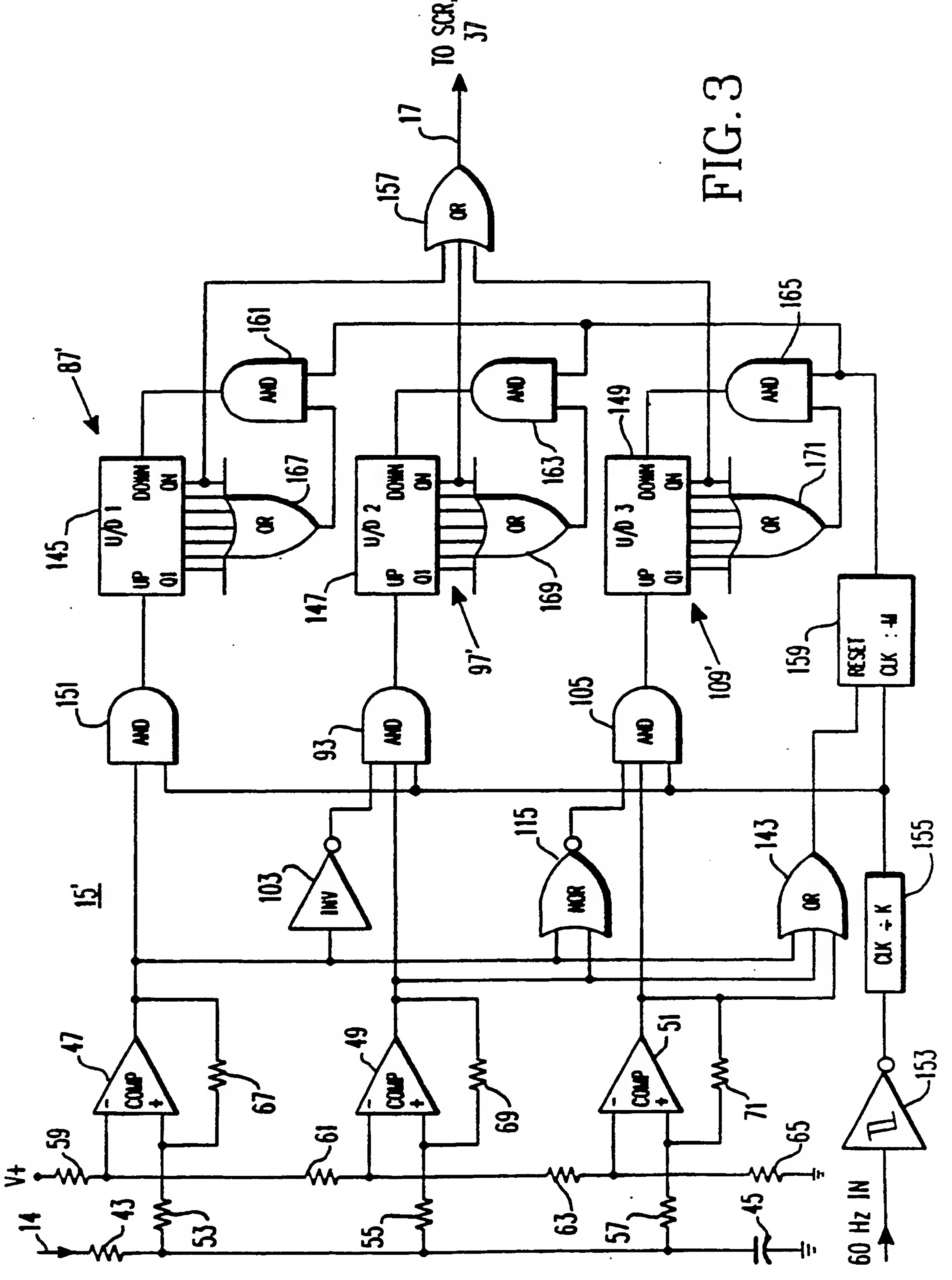

TO SCR, 37
17
157
OR
87'
161
AND
165
145
U/D 1
UP
Q1
DOWN
QN
167
OR
147
U/D 2
163
169
97'
149
U/D 3
171
109'
151
93
105
159
RESET
CLK ÷4
15'
103
INV
115
NOR
143
155
CLK ÷ K
47
COMP
49
51
67
69
71
153
V+
59
61
63
65
14
43
53
55
57
45
60 Hz IN

FIG. 3

?2(r?L?

CIRCUIT BREAKER WITH PROTECTION AGAINST SPUTTERING ARC FAULTS

This invention relates to circuit breakers and more particularly to a circuit breaker with an electronic trip unit which responds to sputtering arc-type faults.

Conventional residential circuit breakers have a thermal trip device which responds to persistent overcurrents of moderate magnitude to provide a delayed trip and a magnetic trip device which responds instantaneously to overcurrents of large magnitude. Thus, the fault current must reach a predetermined magnitude, for example, ten times rated current, for the instantaneous trip to occur, or the overcurrent must sustain a predetermined average value over a given time interval to implement the delayed trip.

There is a type of fault, however, which may not produce either the peak magnitude required for the instantaneous magnetic trip, or the sustained average overcurrent necessary for the delayed trip, yet it may pose a fire hazard. This is the intermittent or sputtering arc-type of fault. Such a fault can occur, for instance, between two conductors that are in close proximity, but not touching, so that an arc is struck between the conductors. This arc can produce a temperature high enough to melt the copper in the conductor. The melted droplets of copper can ignite flammable materials in the vicinity. However, the resistance of the wiring may be high enough to limit the peak current and the ac current cyclically passes through zero to extinguish the arc so that the average current is low.

Thus, the conventional circuit breaker does not respond to the fault, although a hazard exists. This is especially true in the case of a stranded wire extension cord where an individual strand can be melted at a relatively low fault current.

As sufficient voltage is required to strike the arc of a sputtering arc fault, this type of fault typically occurs at the peak of the ac voltage waveform thereby resulting in a step increase in current. Switching of some residential loads also produces step increases in current. For instance, an iron which is turned on at the peak of the voltage waveform results in a step increase in current; however, the magnitude of the step is less than the rated current of the circuit breaker. In addition, inrush currents, such as those produced by the starting of a motor, also rise rapidly, although not as rapidly as an arc-type fault. Furthermore, inrush currents tend to decay exponentially while faults maintain a constant high value, or drop to zero in the case of a sputtering arc.

According to the present invention, a circuit breaker providing fault protection for an electric circuit, said circuit breaker comprising sensing means providing a sensed signal which is a function of current in said electric circuit, detector means comparing the sensed signal with a plurality of threshold levels ranging from a selected high level to a selected low level, timer means generating a trip signal when said sensed signal exceeds any one of said threshold levels for an associated timing interval, trip means responsive to said trip signal opening said electric circuit, in which said threshold levels and timing intervals are selected to produce a response envelope for generation of said trip signal which approximates with a selected margin current in said electric circuit produced by switching into said electric circuit a selected inductive load.

Conveniently, the threshold levels and timing intervals are selected to approximate, with a selected margin, a response envelope for generation of the trip

signal which approximates, with a selected margin, the response of the protected circuit to a selected inductive load. When the sensed signal falls below a previously exceeded threshold, the accumulated time that the sensed signal was above that level is retained, so that if the overcurrent again reaches that threshold level, timing is resumed from where it left off. Thus, as in the case of a sputtering arc fault, where the current can drop off and rise again, a trip signal will be generated when the total selected time for that threshold level has been exceeded even though the current can intermittently fall below that level. The timing intervals are reset when the sensed signal falls below the lowest threshold level. Even then, the intervals are cleared at a very slow rate so that if the current again exceeds one of the thresholds, the interval will be shorter before a trip is generated.

The invention will now be described, by way of example, with reference to the accompanying drawings in which:

Figure 1 is a schematic diagram of a circuit breaker shown in relation to a protected electric circuit.

Figure 2 is a schematic circuit diagram of one embodiment of a detector circuit which forms a part of the circuit breaker shown in Figure 1.

Figure 3 is a schematic circuit diagram of another embodiment of the detector circuit which forms a part of the circuit breaker shown in Figure 1.

Figure 1 illustrates a circuit breaker 1 for protecting a one phase electrical system 3 which includes a line conductor 5 and a neutral conductor 7 energized by a 60 Hz source 9. The circuit breaker 1 includes a sensor 11 for sensing current in the line conductor 5. The sensor 11 is a di/dt sensor which senses the rate of change of the current in the line conductor 5. A suitable di/dt sensor is a mutual inductor having a low permeability core, such as an air core or a powdered iron core. The sensed di/dt signal is full wave rectified in the bridge circuit 13 with the resultant pulsed dc signal applied to a detector

circuit 15 through lead 14 connected to the dc terminals of bridge 13. The detector circuit 15 compares the rectified sensed signal to a number of reference signals and times the intervals that the sensed di/dt signal remains above each of these thresholds. If the rectified di/dt signal remains above any of the reference signals for the associated interval, a trip signal is generated on a lead 17 which is connected to a trip circuit 19.

The trip circuit 19 includes a trip solenoid 21 which when energized opens circuit breaker contacts 23 to disconnect the protected portion of the electrical system 3 from the ac source 9. The trip solenoid 21 is energized from the protected electrical system 3 through lead 25 and is controlled by control circuit 27 which is energized by a bridge circuit 29 connected in series with the trip solenoid 21 by the lead 25.

The control circuit 27 includes a silicon controlled rectifier (SCR) 31 connected across the dc terminals of the bridge 29. The gate of the SCR 31 is connected to the lead 17 from the detector circuit 15. Capacitors 33 and 35 protect the SCR from high frequency spikes.

A zener diode 37 energized by bridge 29 through current limiting resistor 39 generates a V+ reference voltage for the detector circuit 15. Capacitor 41 is a filter.

When the circuit breaker is closed closing the contacts 23, the capacitor 33 charges. This charging current is insufficient to energize the trip solenoid 21. Current drawn by the V+ supply is also insufficient to generate a trip. With the capacitor 35 charged and the SCR 31 off, no appreciable current flows through the trip solenoid 21, and hence, the electrical system 3 remains connected to the ac source 9. When the detector circuit 15 generates a trip signal on the lead 17, the SCR 31 is turned on providing a low resistance path for current which is sufficient to energize the trip solenoid 21 to open the contacts 23. Opening of the contacts 23 deenergizes the

trip circuit 19, however, the circuit breaker contacts 23 remain open until reset.

An analog implementation of the detector circuit 15 is illustrated in Figure 2. In the detector circuit 15, the full wave rectified sensed di/dt signal provided on lead 14 is filtered by an RC filter comprising resistor 43 and capacitor 45. A plurality of level detectors (three in the exemplary embodiment) in the form of comparators 47, 49 and 51 compare the filtered dc di/dt signal to a plurality of reference voltages. The sensed signal is applied to the non-inverting inputs of the comparators 47, 49 and 51 through input resistors 53, 55 and 57, respectively. The reference voltages which are applied to the non-inverting inputs of the comparators are generated by a voltage divider which includes resistors 59, 61, 63 and 65 connected in series between the regulated voltage supply V+ and ground. Feedback resistors 67, 69 and 71 are selected to provide a positive feedback or hysteresis in an amount greater than the magnitude of the ripple on the capacitor 45. Indicators in the form of LED's 73, 75 and 77 are turned on to provide a visual indication when the sensed di/dt signal exceeds the reference voltages applied to the comparators 47, 49 and 51, respectively. Resistors 79, 81 and 83 limit current through these LED's.

The output of the comparator 47 is applied through a diode 85 to a timer 87 formed by the series connected resistor 89 and capacitor 91.

The output of comparator 49 is applied through AND gate 93 and diode 95 to a timer 97 which includes resistor 99 and capacitor 101. The AND gate 93 is controlled by the output of the comparator 47 through inverter 103. Similarly, the output of the comparator 51 is applied through AND gate 105 and diode 107 to a timer 109 which includes a resistor 111 and capacitor 113. The AND gate 105 is controlled by the outputs of both the comparators 47 and 49 through NOR gate 115.

The voltages across the capacitors 91, 101 and 113 are applied through diodes 117, 119 and 121, respectively,

and across a resistor 123 to the non-inverting input of a comparator 125 having a threshold voltage applied to its inverting input by a voltage divider comprising the resistors 127 and 129 and energized by the regulated voltage V+. Each of the capacitors 91, 101 and 113 is also connected through a diode 131, 133 and 135, respectively, to a discharge resistor 137. The outputs of each of the comparators 47, 49 and 51 are ORed in OR gate 143, the output of which is connected to the discharge resistor 137. A resistor 139 and an LED 141 are connected from the output of the OR gate 143 to ground.

The operation of the detector circuit 15 of Figure 2 is as follows. The level of the sensor signal supplied on the input lead 14 is continuously compared with the reference values in the comparators 47, 49 and 51. The outputs of the respective comparators are time delayed by the timers 87, 97 and 109; however, at any given time only the output of the comparator associated with the highest reference voltage which is exceeded is passed through to the respective timer. Thus, if the sensor signal exceeds the reference applied to the comparator 47, AND gate 93 is inhibited through inverter 103 to block timing of the output of comparator 49 and AND gate 105 is disabled through NOR gate 115 to inhibit timing of the output of comparator 51. When the delay selected by the timer 87 has expired so that the voltage across the capacitor 91 minus the forward drop of diode 117 exceeds the reference voltage applied to comparator 125, a trip signal is generated on the output lead 17.

If the sensor signal falls below the threshold of comparator 47 before a trip signal is generated, but remains above the threshold of comparator 49, AND gate 93 is enabled and timer 97 begins timing out. If the sensor signal remains above the threshold of comparator 49 for the selected time interval, the comparator 125 will generate a trip signal.

If the sensor signal falls below the threshold of comparator 49 before the timer 97 times out, but remains

above the threshold of comparator 51 AND gate 105 is enabled by NOR gate 115 and the timer 109 is activated. Again, if this timer times out, a trip signal is generated by the comparator 125.

The delay accumulated in the respective timers is retained as long as the sensor signal remains above the threshold of any of the comparators 47, 49 or 51. This is implemented by the OR 143 which raises the voltage at the junction between the resistors 137 and 139 to prevent discharge of the capacitors 91, 101 and 113 of the timers. Thus, if the level of the sensor signal rises again above the threshold of a higher level comparator, the associated timer picks up timing at the point where it left off, and a trip signal will be generated when the accumulated elapsed time set by the timer has expired. When the sensor signal falls below the threshold of the comparator 51, the timer capacitors are discharged through the resistor 137. The resistor 137 is selected so that the discharge time constant is much larger than the charging time constant so that if overcurrent conditions return, a trip will be generated sooner than for an initial overcurrent condition. The LED's 73, 75 and 77 are turned on when the thresholds of the associated comparators have been exceeded. This provides a visual indication that an overcurrent condition exists which could result in a trip and the relative severity of the overcurrent. The LED 141 provides a redundant indication, when it is energized, that overcurrent conditions exist. Alternatively, only the LEDs 73, 75 and 77 or just the LED 41 could be provided.

The threshold reference voltages of the comparators 47, 49 and 51 and the time constants of the timers 87, 97 and 109 are selected to generate an envelope which approximates the exponential decay of a step function. This envelope can be set so that it exceeds, but follows, the response which would be generated by the introduction of an inductive load, such as the starting of a motor, in the electrical system 3 protected by the circuit breaker. Thus, the circuit breaker would not trip on the starting of

the motor, but would provide short delay response for faults, and would be especially useful for responding to low overcurrent but persistent faults such as sputtering or intermittent arc faults.

Figure 3 illustrates a hybrid analog/digital implementation of the detector circuit. Components in this detector circuit 15′ which are identical to components in the analog circuit of Figure 2 are identified by like reference characters. This circuit 15′ includes digital delay or timer circuits 87′, 97′, and 109′, respectively, associated with the comparators 47, 49 and 51, respectively.

The timers 87′, 97′ and 109′ each include an up/down counter 145, 147 and 149, respectively. Each of the counters 145, 147 and 149 have the number of stages required for the respective time delays. The output of the comparator 47 is applied through an AND gate 151 to the count-up input of the counter 145. Similarly, the outputs of comparators 49 and 51 are applied to the count-up inputs of the counters 147 and 149, respectively, through the AND gates 93 and 105. These AND gates are enabled by clock pulses. The clock pulses are generated from the 60 Hz of the electrical system 3 by a Schmitt trigger 153. Since the delay intervals are long compared with the period of the 60 Hz of the electrical system, the pulses generated by the Schmitt trigger 153, are divided down by a factor of K by divider 155. The last stages of the counters 145, 147 and 149 are ORed by OR gate 157 to generate the trip signal on lead 17 when any of the counters times out.

As in the case of the circuit of Figure 2, only the counter in the circuit 15′ associated with the comparator having the highest threshold which is exceeded counts at any given time. The counters 145, 147 and 149 are reset by clock pulses from divider circuit 159 which divides the clock pulses down further by a factor of M so that the counters are reset at a slower rate than that at which they count up. The reset pulses from the divider 159 are applied through AND gates 161, 163 and 165 to the count-

down inputs of the counters 145, 147 and 149, respectively. These AND gates 161, 163 and 165 are enabled by outputs from OR gates 167, 169 and 171 which OR the bits of the associated counters. Thus, the AND gates 161, 163 and 165 pass pulses from the divider 159 to the count-down inputs of the counters 145, 147 and 149 until the counts reach zero. The OR gates 167, 169 and 171 prevent the counters from rolling over after they reach zero. Reset pulses are generated by the divider 159 only when none of the thresholds of the comparators 47, 49 or 51 are exceeded as determined by the OR gate 143 which holds the divider 159 at reset as long as a threshold of one of the comparators 47, 49 or 51 is exceeded. If desired, indicators such as the LEDs 73, 75 and 77 or the LED 141 can be included in the detector circuit 15′ to provide a visual indication of the level of the overload current or to generally indicate an overload condition.

The electronic trip feature of the invention can be incorporated into a conventional circuit breaker having a magnetic instantaneous and a delayed thermal trip, such as the circuit breakers disclosed in United States patent Nos. 3,858,130; 3,999,103 or 4,081,852 which are hereby incorporated by reference. The present invention provides protection against faults such as sputtering arc faults in which the overcurrent is less than that required for an instantaneous magnetic trip, but greater than that required for a thermal trip. The additional components required by the invention are housed in the half of the circuit breakers of these patents housing the trip solenoid, and are connected to the trip solenoid which when energized rotates a lever extending through a partition to actuate the trip mechanism in the other half of the housing.

IDENTIFICATION OF REFERENCE NUMERALS USED IN THE DRAWINGS

LEGEND	REF. NO.	FIGURE
DETECTOR CIRCUIT	15	1
- COMP +	47	2
- COMP +	47	3
- COMP +	49	2
- COMP +	49	3
- COMP +	51	2
- COMP +	51	3
AND	93	2
AND	93	3
INV	103	2
INV	103	3
AND	105	2
AND	105	3
NOR	115	2
NOR	115	3
- COMP +	125	2
OR	143	2
OR	143	3
U/D 1 UP DOWN Q1 QN	145	3
U/D 2 UP DOWN Q1 QN	147	3
U/D 3 UP DOWN Q1 QN	149	3
AND	151	3
CLK ÷ K	155	3
OR	157	3
RESET CLK : -M	159	3
AND	161	3

IDENTIFICATION OF REFERENCE NUMERALS USED IN THE DRAWINGS

LEGEND	REF. NO.	FIGURE
AND	163	3
AND	165	3
OR	167	3
OR	169	3
OR	171	3

CLAIMS:

1. A circuit breaker providing fault protection for an electric circuit, said circuit breaker comprising sensing means providing a sensed signal which is a function of current in said electric circuit, detector means comparing the sensed signal with a plurality of threshold levels ranging from a selected high level to a selected low level, timer means generating a trip signal when said sensed signal exceeds any one of said threshold levels for an associated timing interval, trip means responsive to said trip signal opening said electric circuit, in which said threshold levels and timing intervals are selected to produce a response envelope for generation of said trip signal which approximates with a selected margin current in said electric circuit produced by switching into said electric circuit a selected inductive load.

2. A circuit breaker as claimed in claim 1 wherein said timer means at any given time only times the highest threshold level exceeded.

3. A circuit breaker as claimed in claim 2 wherein said timer means retains accumulated time for a threshold which has been exceeded when said sensed signal falls below that threshold level, and picks up timing at the accumulated time if that threshold is again exceeded, and in which said timer means includes means clearing all time intervals when said sensed signal falls below said selected low level.

4. A circuit breaker as claimed in claim 1 wherein said sensing means generates a sensed signal

representative of the rate of change of current in the electric circuit.

5. A circuit breaker as claimed in any one of claims 1 to 4 including instantaneous magnetic trip means responsive to current in said electric circuit greater than represented by said selected high level operating said trip means to open said electric circuit, and thermal trip means responsive to a persistent current in said electric circuit at a second selected magnitude lower than that represented by said selected low level operating said trip means to open said electric circuit.

6. A circuit breaker as claimed in claim 1, wherein a plurality of level detectors each detecting a different level of said sensed signal from a selected high level to a selected low level, a plurality of timer means each associated with a different level detector and each having a selected timing interval which times out and generates a trip signal when the associated level detector has detected the assigned level of said sensed signal for the selected timing interval, and trip means responsive to said trip signal generated by any of said timer means opening said electric circuit.

7. A circuit breaker as claimed in claim 6 including means freezing said timer means associated with detectors for which the sensed signal has fallen below the threshold level of the associated level detector, until said sensed signal again exceeds the threshold level of the associated level detector, including means clearing each of said timer means when the sensed signal falls below said selected low level.

8. A circuit breaker as claimed in claim 7 wherein each of said timer means comprises a series resistor-capacitor circuit, said means clearing each timer means comprises a discharge path for said capacitors, and said means freezing said timer means comprises means blocking said discharge path.

9. A circuit breaker as claimed in claim 8 wherein said clearing means comprises discharge resistor

means and diode means connecting each of said capacitors for flow of current only from said capacitors to said discharge resistor means, and wherein said means blocking discharge of said capacitors comprises means responsive to the sensed signal exceeding the threshold level of any level detector to raise the voltage on said discharge resistor to reverse bias said diode means.

10. A circuit breaker as claimed in claim 9 wherein said timer means each equal an up/down counter and means applying pulses to said counter to count up when the threshold level of an associated level detector is exceeded, wherein said clearing means comprises means applying pulses to said counters to count down, and wherein said means freezing said timers comprises means blocking the application of pulses to said counters to count down when the sense signal is above the threshold level of any of said level detectors.

Patents Act 1977
Examiner's r port to the Comptroller under Section 17 (The Search Report)

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Relevant Technical fields

(i) UK Cl (Edition K) H2K (KHB, KJE, KJG)

(ii) Int Cl (Edition 5) H02H (3/093)

Databases (see over)

(i) UK Patent Office

(ii)

Search Examiner

P NICHOLLS

Date of Search

11 NOVEMBER 1992

Documents considered relevant following a search in respect of claims 1-10

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
P, X	GB 2244183 A (PLESSEY) 20 November 1991, Figure 2	1 at least
X	GB 2020124 A (TSDKK) page 5 lines 1-19	1 at least
X	GB 1594112 A (WESTINGHOUSE) page 1 line 71 page 2 line 37	1 at least
X	GB 1069626 A (ENGLISH ELECTRIC) whole document	1, 6 at least
X	EP 0253009 A1 (MITSUBISHI) column 2 lines 25-51	1 at least
X	EP 0245819 A2 (LITTON) Figures 2 and 3	1, 6 at least
X	US 4000446 A (VANDEVIER) Figure 5	1, 6 at least

Category	Identity of document and relevant passages	Relevant to claim(s.

Categories of documents

X: Document indicating lack of novelty or of inventive step.

Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family, corresponding document.

Databases: The UK Patent Office database comprises classified collections of GB, EP, WO and US patent specifications as outlined periodically in the Official Journal (Patents). The on-line databases considered for search are also listed periodically in the Official Journal (Patents).

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